DC/DC Converter
AC/DC Inverters
Delay-Lines
Pulsetransformers
Burst & Surge Filters
Hamonic Filters
Switching Power Supplies

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FLOETH ELECTRONIC

AN5706-2.0 May 2004

HV2-15 Industrial Series

IGBT Driver Module Application Note

FEATURES

- Suitable for Existing Interface Cards
- Protects IGBT from Short Circuit Failure
- High Reliability
- Gate Current to ±15A
- Electrical Isolation min. 10kV AC rms
- Partial Discharge Free Upto 2300V AC rms
- Supply Voltage Monitoring
- Switching Frequency DC to 100kHz
- Limitation Input Current 800mA at 15V IN
- Duty Cycle 0 to 100%
- Built-in Isolated DC/DC Power Supply

APPLICATIONS

- Industrial Drives
- Multi Level Converters
- Railway Traction Drives and Auxiliaries
- Power Supplies
- Wind Turbines

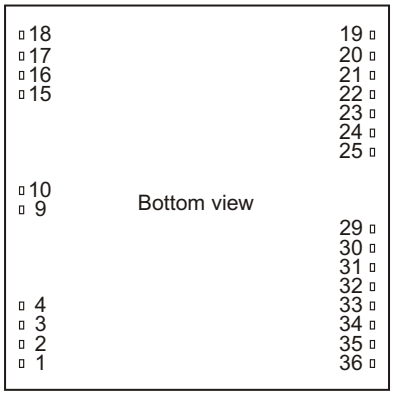
This application note features an IGBT driver solution designed and manufactured by Floeth Electronic. The HV2-15 is compact single channel intelligent gate drive module which in combination with the appropriate interface board can be used to drive high power IGBT modules from major manufacturers. The module incorporates a DC/DC power supply and features functional options selectable via jumpers on the Interface Card.

Complete driver solutions consisting of these modules mounted on suitable interface boards are available. For further information please contact Floeth Electronic via floeth-electronic@t-online.de

The information presented herein is provided in good faith but it is the users responsibility to determine the performance suitability of this drive solution in any actual application

KEY PARAMETERS

Drive Voltage	**±15V**
Drive Power	**±3W Total 6W**
Gate Drive Current	**±15A**
Logic Input/Output	**5V**
Ref. Voltage	**15V**



(See package details for further information)

Fig. 1 Electrical connections - (not to scale)

ORDERING INFORMATION

Order As:

HV2-15

2300V AC rms partial discharge free

Note: When ordering, please use the complete part number.

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed. Exposure to Absolute Maximum Ratings may affect device reliability.

T_{case} = 25˚C unless stated otherwise

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{DC}	Supply voltage	V_{DC} to GND	0	15.75	V
I_{OUT}	Gate peak output current	-	-	±15	A
V_{logic}	Internal logic supply - linear regulated	-	-	5	V
I_{DC}	Average supply current	No load	-	100	mA
$I_{DC(max)}$	Maximum supply current	-	-	800	mA
P_{OUT}	Output power DC/DC converter	-	1	6	W
f	Switching frequency	Depending on load characteristics	-	100	kHz
V_{ISOL}	Isolation voltage	AC RMS 1 min.	-	10	$kV_{AC(RMS)}$
V_{REF}	Internal reference voltage	Line regulated	-	15	V
T_{amb}	Ambient temperature range - Industrial - HV2-15	-	–40	+71	˚C
T_{stg}	Storage temperature range	-	–55	+90	˚C

ELECTRICAL CHARACTERISTICS - POWER SUPPLY

T_{case} = +25˚C and V_{DC} = 15V unless stated otherwise

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{DC}	Nominal supply voltage	V_{DC} to GND	14.25	15	15.75	V
UVLO	Undervoltage lockout	Internally generated, I_L = 60mA	-	13	-	V
I_{DC}	Supply current	Zero load	-	-	150	mA
P_{MOD}	Power consumption of driver module	15V supply, zero load	-	2.25	-	W

ELECTRICAL CHARACTERISTICS - LOGIC INPUTS

T_{case} = +25˚C and V_{DC} = 15V unless stated otherwise

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{INH}	Input H-level voltage	-	3.8	-	-	V
V_{INL}	Input L-level voltage	-	-	-	0.8	V

ELECTRICAL CHARACTERISTICS - ELECTRICAL ISOLATION

T_{case} = +25˚C and V_{DC} = 15V unless stated otherwise

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{TEST}	Test voltage - Primary to output	50Hz / 1 min	-	-	10	$kV_{AC(RMS)}$
V_{ISOL}	Isolation voltage	-	-	-	2.3	$kV_{AC(RMS)}$
-	Creepage distance - primary to output	-	-	-	43	mm

ELECTRICAL CHARACTERISTICS - TIMING

T_{case} = +25˚C and V_{DC} = 15V unless stated otherwise

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$t_{d(on)}$	Turn-on delay time	Refer to Figs. 9 and 10	-	550	-	ns
$t_{d(off)}$	Turn-off delay time	Refer to Figs. 9 and 10	-	800	-	ns
$t_{r(out)}$	Output current rise time	Refer to Figs. 9 and 10	-	150	-	ns

BLOCK DIAGRAM

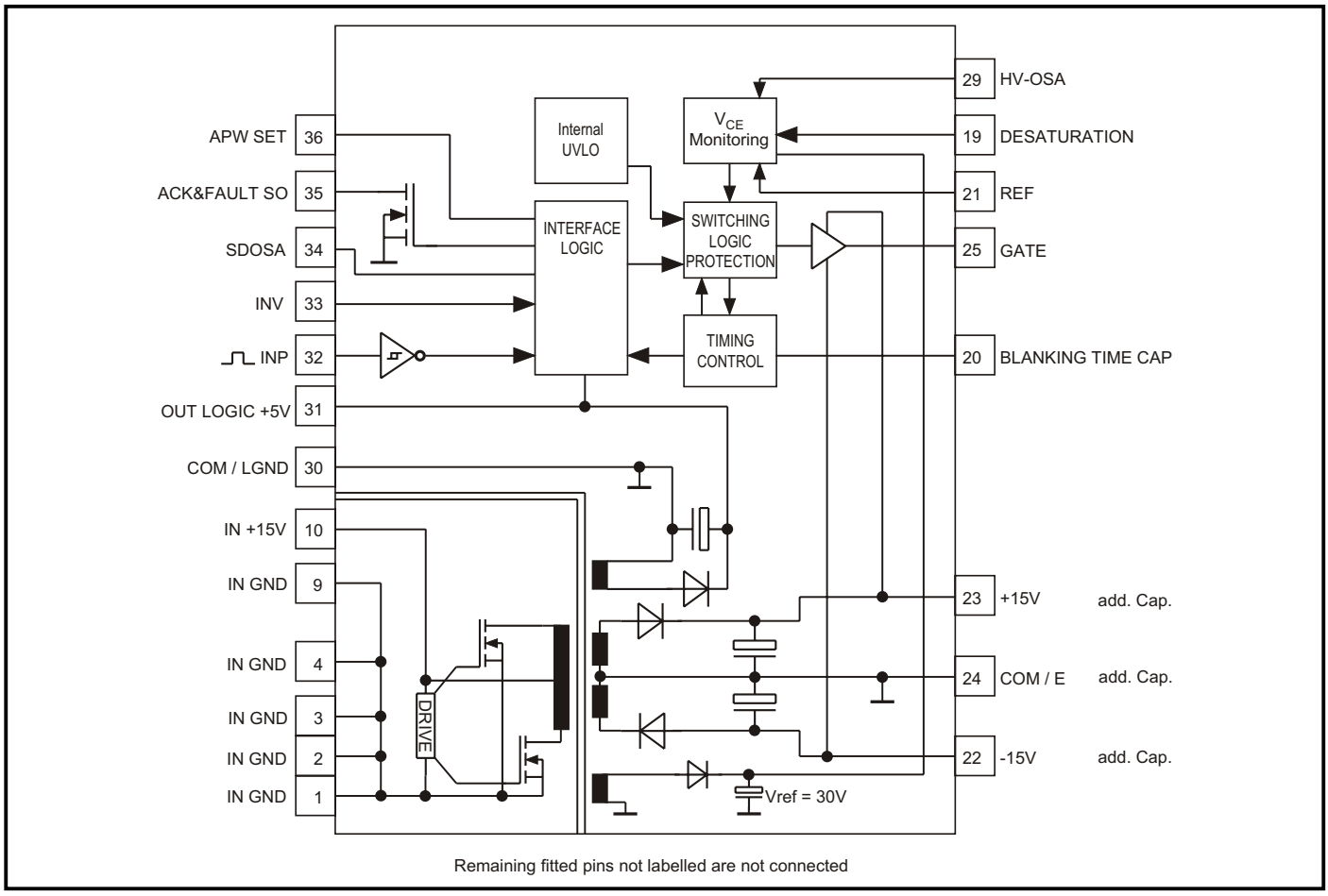


Fig. 2 Module block diagram

PIN CONNECTIONS

Pin No.	Description	Note
1	INPUT GND	
2	INPUT GND	
3	INPUT GND	
4	INPUT GND	
5 to 8	NOT CONNECTED	
9	INPUT GND	
10	INPUT 15V ± 5%	
11 to 18	NOT CONNECTED	
19	V_{CE} / DES	Monitoring input with reference to COM, to be connected to sense capacitor and then to collector of power switch via fast HV diode and resistor.
20	BLANKING TIME CAPACITOR (BTC)	Value determines time ACK signal remains Low after removal of fault condition.
21	REF Voltage Pin	Level to be adjusted to suit actual IGBT. V_{CE}/DES in turn ON mode, to be set by appropriate Zener diode or resistors. Internal Ref. voltage is 30V which allows VCE / DES to be monitored up to 28V approx. For higher V_{CE}/DES an Extended Ref. Voltage Module (ERVM) is available which can provide a V_{REF} up to 200V.
22	–15V Supply voltage	Decoupling capacitor required.
23	+15V Supply voltage	Decoupling capacitor required.
24	COM / E	Secondary side common / Power switch emitter connection point.
25	Gate drive power output	Connect via gate resistor or gate resistor/diode combination with short wire length.
26 to 28	NOT CONNECTED	
29	HV-OSA	Out of saturation activation pin - normally connected to COM. For higher V_{CE}/DES an ERVM must be used - consult Dynex or Floeth.
30	LGND/COM	GND for all small signal and logic connections
31	+5V LOGIC SUPPLY	From internal converter
32	SIGNAL INPUT	Connect to FOL - Receiver
33	INPUT/OUTPUT REVERSAL	Input Low (connected to pin 30 LGND/COM): Gate Output (pin 25) is antiphase to Input (pin 32). Input High (open): Gate output (pin 25) is in phase to input (pin 32).
34	SDOSA	Shutdown out of saturation - two options. 1. Normally pin 34 pulled to COM - in this condition the driver turns the the IGBT off immediately and reports fault to control unit via SO. 2. Set to +15V, at fault the driver does not turn off the IGBT, but reports the fault immediately to the control unit, (which may subsequently turn off all the IGBTs in the system at once).
35	ACK&FAULT SO	Open drain output - 220 Ohms used as pull up resistor to 5V connect to FOL transmitter (Fibre Optic Link) transmitter LED
36	ACK PULSE WIDTH (APW) SET	Capacitance from this point to COM determines pulse width, e.g. 56pF gives approx. 1.2µs, but should be as lower value as is possible.

INTRODUCTION

The HV2-15 offers a complete solution for driving and protecting IGBT modules and only a few additional components are required in the control circuit and in the power section.

The HV2-15 is suitable for high frequency switching up to 100kHz.

This module may also be used in conjunction with other manufacturers' interface cards. Please contact Floeth Electronic for further information.

RELIABLE OPERATION

A gate voltage between ±14V to ±16V ensures reliable operation of IGBT modules. High noise immunity is achieved with the negative gate voltage, and a number of IGBTs may be connected in parallel without problems from parasitics.

The module incorporates short circuit protection for the IGBT, supply monitoring, status acknowledgement, and an electrically isolated supply for the drive electronics.

SHORT CIRCUIT PROTECTION

One of the fundamental functions of the driver module is to ensure reliable protection of the controlled IGBT against short circuit and over current. The current measurement is based on collector-emitter voltage of the IGBT in the on-state. Once the predetermined threshold has been exceeded the IGBT is turned off and remains 'blocked' in normal mode for a minimum predetermined time. Once this period has elapsed the IGBT is released and may be switched again.

This is a simple and reliable method of protection for the IGBT removing the requirement for additional components.

PIN DESCRIPTIONS

Pins 1, 2, 3, 4, 9 and 10 GND and V_{CE}

The nominal feed on the power supply pins is between 15V ± 5%. For reliable operation of the integrated DC/DC converter a low impedance, high ripple current rated electrolytic capacitor must be positioned in the immediate vicinity of Pins 9 and 10. The capacitance of this component should typically be the same value as the capacitor connected to Pin 23. The DC/DC converter current consumption is dictated by the number of IGBTs in parallel being driven, their gate capacitance and by the switching frequency.

The module will operate from a 12V supply if a gate drive voltage lower than the standard 15V is required. This may be useful when driving IGBTs that have high saturation currents under short circuit conditions. However, please note that the driver module is not protected against overload and a short circuit between the gate and emitter terminal may lead to thermal destruction of the internal components.

Pin 19 - V_{CE} / DES Monitor

This is used to monitor the voltage drop across the collector-emitter of the controlled IGBT at turn-on in order to detect a short circuit condition. **Note: Do not connect directly to the auxiliary collector of the IGBT.** To block the high collector voltage that is present when the IGBT is turned off, a high voltage diode (or several diodes) must be connected in series. The voltage rating of these diodes must exceed the maximum voltage seen at the IGBT collector in transient turn-off conditions.

A voltage source in the driver module ensures that current flows through the measurement diodes (D1 to D3), the attenuation resistor (Rs) and the IGBT at turn-on. The function of Rs is to attenuate spikes caused by reverse recovery of diodes D1 to D3. Typically Rs has a value of 68Ω.

When the IGBT is turned on, the potential present at the measurement input of V_{CE} / DES corresponds to the forward voltage of the IGBT plus the forward voltage of the diodes and the voltage drop across Rs.

The integrated voltage source and an external capacitor, (C_{sense}), produces a measurement delay after the IGBT has switched on. This delay is known as the 'response time' and C_{sense} must be selected to provide a delay greater than the turn-on time of the IGBT.

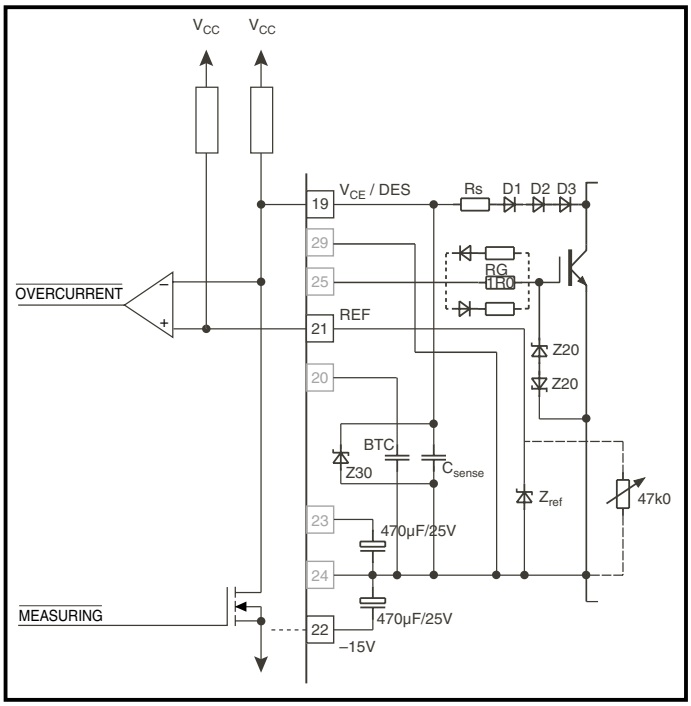


Fig. 3 V_{CE} monitoring

$$C\ (pF) \sim \left\{ \frac{(\text{Response time (ns)} - 600\text{ns})}{(33\ln [14.945 / (15V) - V_{pin21}\ (V)]} \right\} - 30 \quad \textbf{[1]}$$

The response time may be adjusted by varying the value of C_{sense}. Z30 is connected in parallel to C_{sense} to protect the module against damage in case of excessive V_{CE}. Z15 should not be used if V_{CE} in turn-on mode is greater than 28V.

Note: Negative voltages are not permissible at this pin.

Pin 20 - Blanking Time Capacitor (BTC)

Once the current monitoring circuit has detected that the IGBT is in a desaturation state, the IGBT is turned off in normal mode by the driver module's protection function and remains in this state until overload is removed. This function is used to protect the IGBT from thermal overload during continuous or repeated short circuits. An error signal on status output SO appears for the duration of the blanking time. The blanking time is determined by connecting Pin 20 (BTC) to Pin 24 (COM) via a capacitor.

BTC value = C (nF) ~ 14.064 x t (msec.) **[2]**

The value of BTC typically is 470nF. After the blanking time has elapsed the IGBT is immediately released for operation.

Pin 21 - Reference Voltage, REF

The external zener diode connected to this pin defines the voltage drop across the driven IGBT at which the desaturation detection function of the drive circuit is activated.

The protection function becomes active when the voltage at Pin 19 (V_{CE} / DES Monitor) is higher than that at REF.

The reference potential is the emitter of the IGBT. The reference zener diode must be positioned as close to the driver module as possible.

Pin 22 - –15V

A low impedance, high ripple current rated electrolytic capacitor is connected at Pin 22. This de-couples the DC/DC converter on the secondary side. The capacitor must supply the pulses of current that discharge the IGBT gate capacitance. The capacitor is connected between Pin 22 and Pin 24 (COM). As the discharging currents for the gate are drawn mainly from the capacitor it is imperative that it is positioned as near to the driver module as is physically possible. The recommended value for the capacitor is 470µF. Values significantly greater than this may prevent the DC/DC converter from starting at power-up.

If flying leads are used between the driver module and the IGBT emitter or drain terminals then their length should not exceed 100mm. The leads should run to each IGBT in twisted form.

Pin 23 - +15V

A low impedance, high ripple current rated electrolytic capacitor is connected at Pin 23. This de-couples the DC/DC converter on the secondary side. The capacitor must supply the pulses of current that charge the IGBT gate capacitance. The capacitor is connected between Pin 23 and Pin 24 (COM). As the charging currents for the gate are drawn mainly from the capacitor it is imperative that it is positioned as near to the driver module as is physically possible. The recommended value for the capacitor is 470µF. Values significantly greater than this may prevent the DC/DC converter from starting at power-up.

Pin 24 - Power Switch Emitter, COM

This pin should be connected directly to the IGBT emitter terminal (or auxiliary emitter terminal where available) using as short a lead as possible. It is also used as the zero voltage reference point for reference voltage REF.

This is the signal ground of the secondary side isolated power supply. It is used as the reference potential for the desaturation detection filter and the power supply de-coupling capacitors. (See Fig. 4).

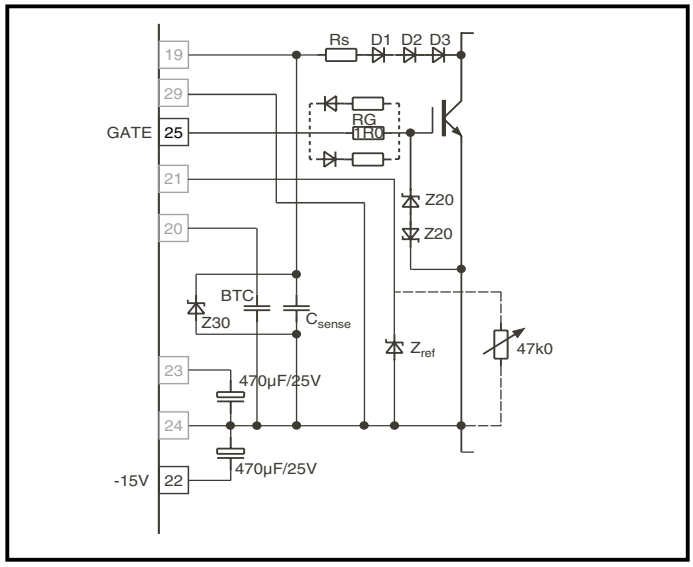


Fig. 4 Asymmetrical gate resistors

Pin 25 - Output Gate

This is the driver output for the IGBT gate. Depending on the module supply voltage, potentials are usually in the range of ±12V to ±15V.

The output stages of the HV2-15 series has a maximum possible gate charging current of ±15A. The charging current can be limited by an external gate resistor. Remember that when the gate is driven with an alternating voltage symmetrically around zero, the potential difference across the gate capacitance is double the on-state gate voltage.

During IGBT turn-off the Miller effect may cause the gate voltage to rise and this can delay device turn-off. It is advisable to connect zener diodes (Z20, Z21) immediately between the IGBT gate and emitter to clamp the gate voltage to a predetermined level. This should be just greater than the normal gate enhancement voltage.

The gate of the IGBT must be connected to Pin 25 by a lead as short as possible. Using a gate circuit of two resistors and a diode the turn-on and turn-off switching speeds can be set independently of each other. (See Fig. 5).

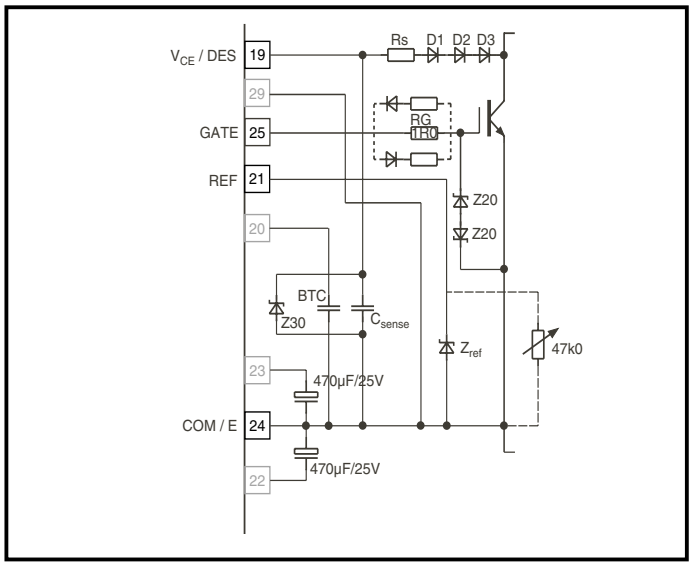


Fig. 5 Asymmetrical gate drive

Pin 29 - HVSOA

Out of saturation activation pin connected to COM (Pin 24) for standard operation. Reference voltages greater than 15V can be implemented with additional circuitry, consult Floeth Electronic.

Pin 30 - LGND/COM

Ground for all small signal and logic connections. (See Fig. 6).

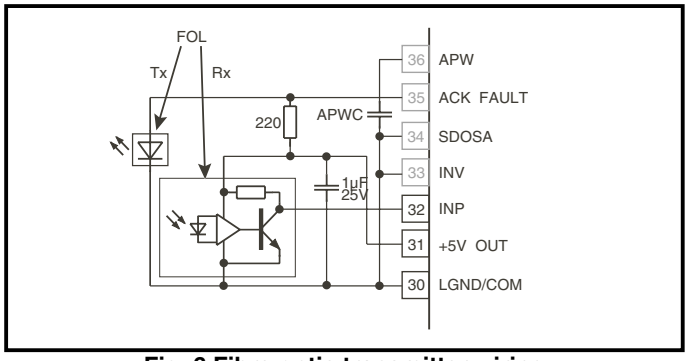


Fig. 6 Fibre optic transmitter wiring

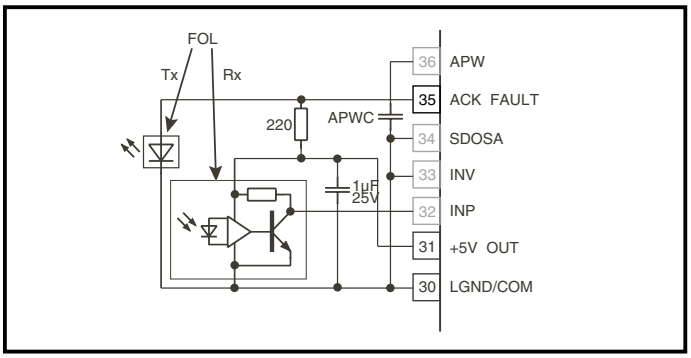


Fig. 7 Fibre optic receiver wiring

Pin 31 - +5V Logic Supply, LGND

+5V with respect to LGND is available from this pin which is intended to supply the interface electronics, specifically the Fibre Optic Link (FOL) receiver. (See Fig. 7). The maximum current capability of 60mA for this output must not be exceeded. If an FOL receiver requiring more than 60mA is used then an external 5V controller should be connected which can be supplied via Pin 23.

Pin 32 - INPUT Signal

The output signal of the FOL receiver is applied to this terminal. For recommended receiver see page 10. The INPUT terminal has a Schmitt trigger characteristic to provide improved signal-to-noise immunity. The logic sense of the INPUT terminal may be inverted by Pin 33 INV (INPUT/OUTPUT Reversal). With INV connected to LGND, a 5V signal at INPUT corresponds to “IGBT ON”, and a 0V signal to “IGBT OFF”. If INV is open, INPUT works in the opposite sense.

Pin 33 - INV

This pin allows the sense of input signal INPUT to be inverted.

Pin 33 is internally pulled high when not ocnnected to LGND. Pin 33 can be pulled to LGND by closing J2 on the interface card.

Pin 34 - SDOSA

Used to select the response of the protection function. In normal operation, the SDOSA terminal is tied to COM with the consequence that when a fault (in the desaturation or supply voltage monitoring circuits) is detected, the IGBT is immediately turned off, even if the input signal continues to be applied. The fault situation is simultaneously reported via the status output, (ACK/FAULT).

The alternative operating mode is useful when driving IGBTs connected in series. In this mode the SDSOA input is connected to +15V. When a fault is detected by desaturation the IGBT is not turned off. The SO, Status Output or ACK/FAULT Pin 35 goes low (error flag) and reports to the central microcontroller to turn-off all the series IGBTs simultaneously.

The same approach may also be used for IGBTs connected in parallel but each having a dedicated driver. In this situation, symmetrical current distribution is maintained by simultaneous turn-off of the drivers. The driver module is therefore suitable for any combination of series or parallel IGBTs and is also applicable to bridge circuits.

In the event of a fault it is important in each case that the status acknowledgements are detected quickly and as directly as possible. These signals should be monitored by a dedicated circuit such as a PAL or FPGA and not by a microprocessor which may take too long to react.

Pin 35 - SO, Acknowledge Fault Status Output

This is the driver status output. This signal can be relayed back to a central controller via an isolating FOL. (See Fig. 7). The +5V supply for the FOL transmitter is taken from pin 31.

SO has the following states:

If the driver module supply voltage is within specification and there is no other fault condition then an acknowledge (SO) pulse is transmitted even if the blanking time is high.

If the protection function of the driver detects desaturation, terminals 30 and 35 are shorted together for the duration of the blanking time. SO is pulled low.

SO also indicates every switching edge of the IGBT driving signal with a short SO pulse, (during which the FET conducts). The length of the SO pulse is determined by the capacitor (APWC) connected to Pin 36. The SO function allows the control electronics to continuously monitor the operation of the driver and status acknowledgement functions.

If the SO pulse is low for longer than usual then the control electronics may assume that there is a problem with the FOL. **Incorrectly installed FOL connections may have catastrophic results.** An SO pulse must be present at SO at every edge of the input signal.

Floeth Electronic recommends that the status acknowledgements from several drivers are not connected together, but are evaluated as individual signals by a monitoring circuit. This simplifies troubleshooting and diagnosis in the event of a fault.

Pin 36 - Acknowledge Pulse Width Set, APW

The length of the SOK pulse (approx 1.2µs) on the SO output is determined by a 56pF capacitor connected between APW and Pin 24 (COM). The optimum pulse length should be as short as possible.

The SO pulse is approximately 300ns if a capacitor is not connected to Pin 36.

POWER SECTION - CONFIGURATION

The driver module should be positioned as close as possible to the controlled IGBT with connection leads not more than 30 to 100mm in length, depending on the gate current and switching speed. The FOL cable lengths are not critical.

GATE RESISTOR - R_G

R_G determines the maximum gate current and protects the power switch and the driver against permanent damage. A low inductance metal band resistor is recommended.

For example, for type HV2-15

R_G for a gate current of 15A = V_{gate} / $I_{max.}$ driver

= 30 V / 15A = 2.0 Ohm min. **[3]**

Note that any internal gate resistor in the IGBT modules forms part of the charging circuit and must be taken into account when selecting the external gate resistor value. Furthermore, if different turn-on and turn-off gate currents are required, which can be achieved as shown in Fig.8, the combined parallel values

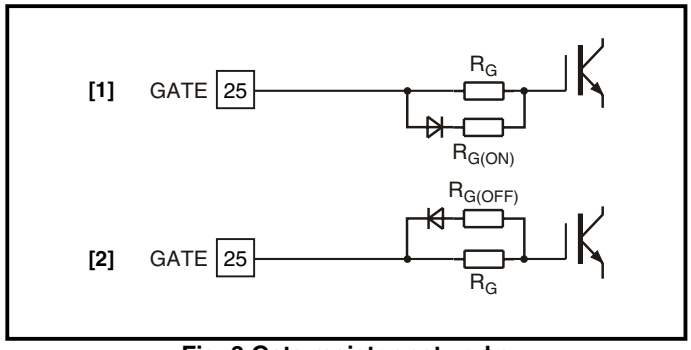


Fig. 8 Gate resistor networks

REFERENCE VOLTAGE - Z_{REF}

The VCE voltage at which overcurrent/short circuit condition is detected is set by the Zener diode connected to pin 21. Pin 34 must be connected to COM. Alternatively, a 47k0 potentiometer may be used to allow easy adjustment.

ACK PULSE CAPACITOR - C_{APW}

C_{APW} ~ 56pF generates approximately 1.2µs.

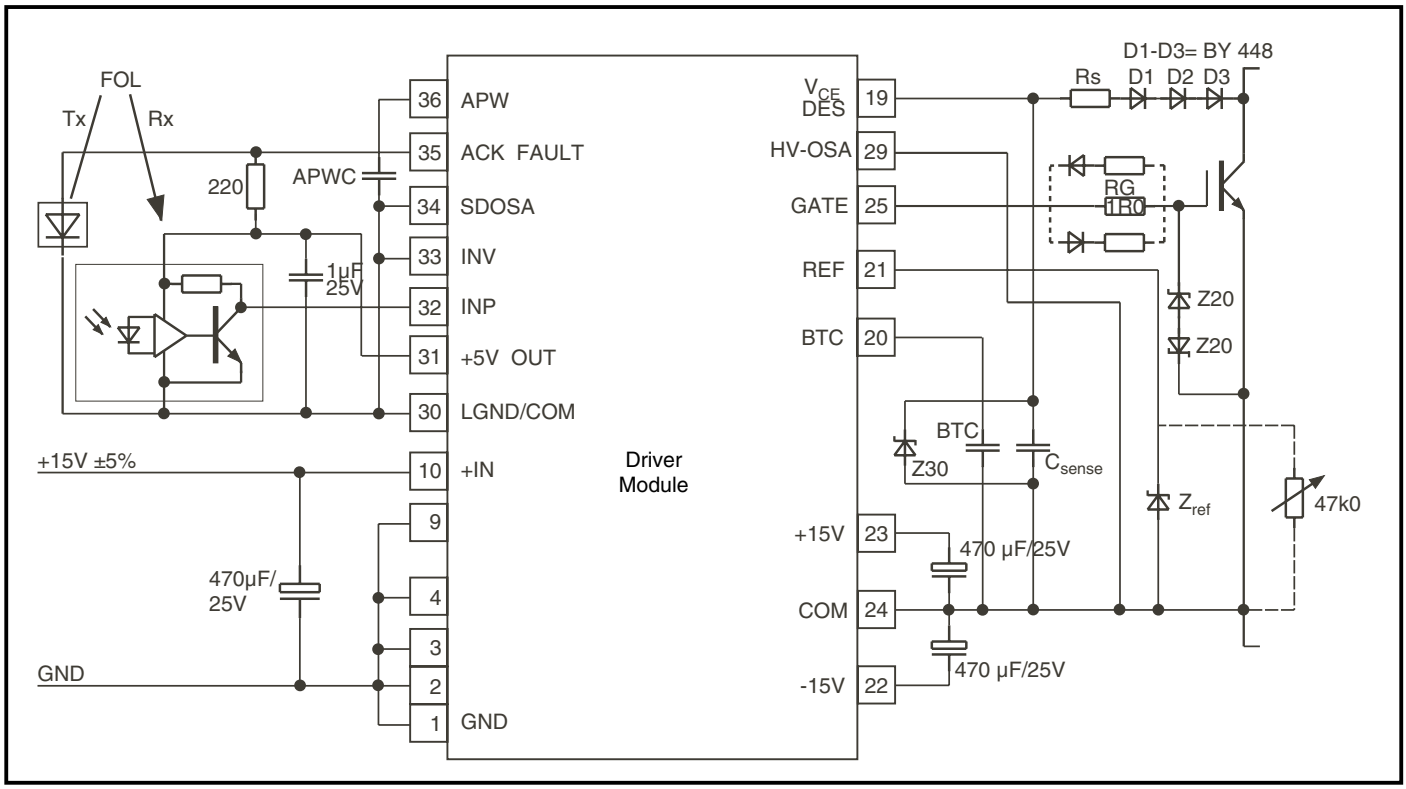


Fig. 9 Example driver circuit

FIBRE OPTIC LINK - RECOMMENDATION

HP/Agilent Transmitter: T-1524

HP/Agilent Receiver: R-2524

TIMING PATTERNS

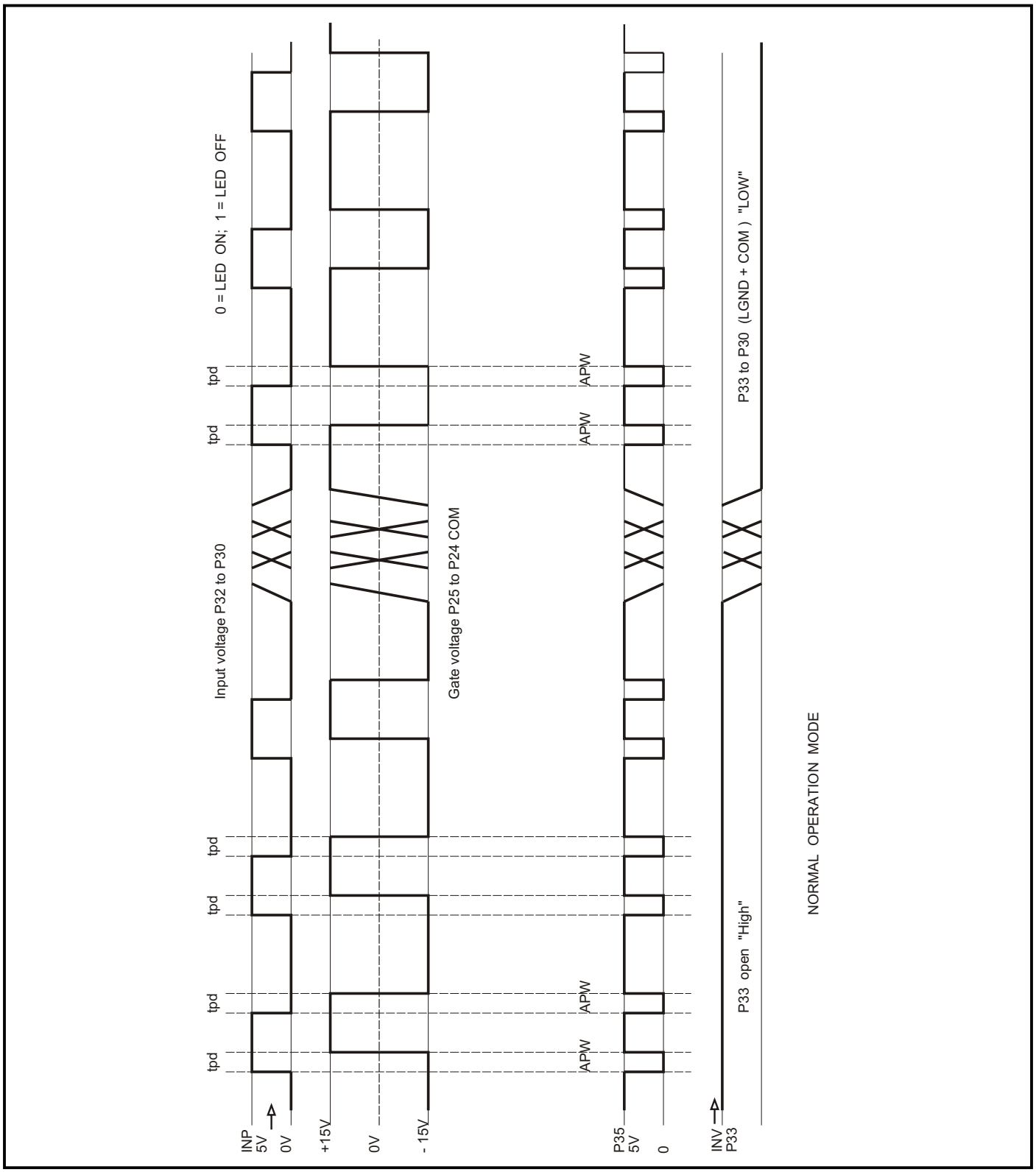


Fig. 10 Signal traces

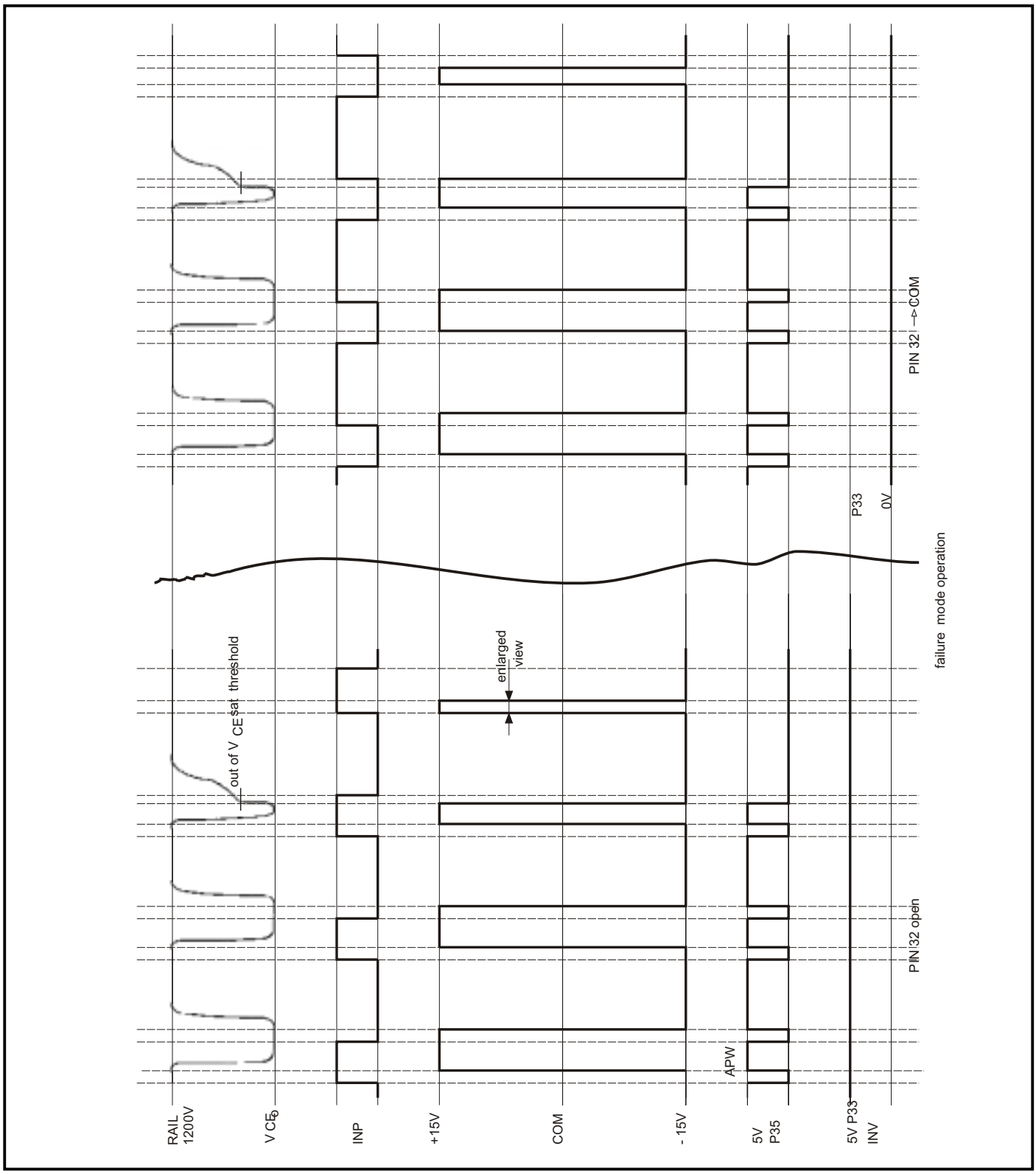
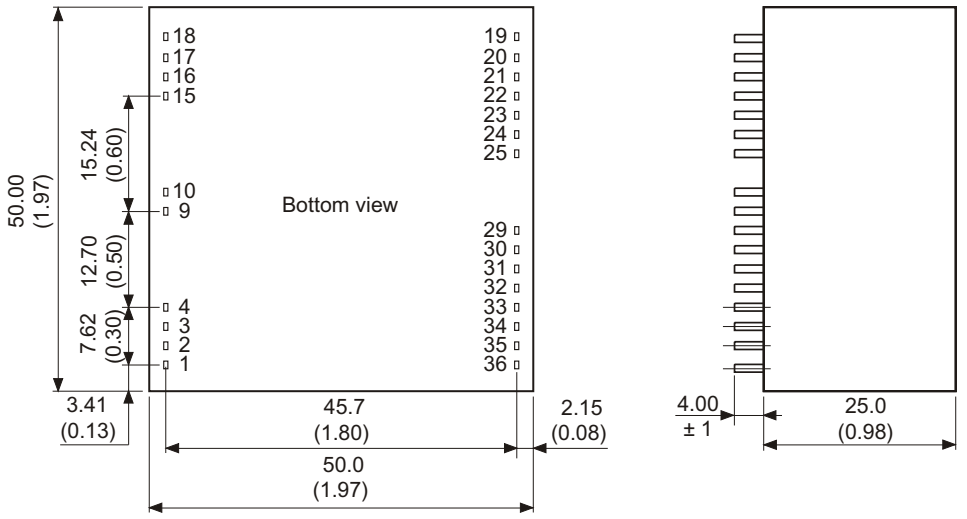


Fig. 11 Signal traces

PACKAGE DETAILS

For further package information, please visit our website or contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



Material information:
Drivers are epoxy moulded within a 50 x 50 x 25mm enclosure.
PCBs and epoxy materials are self-extinguishing in accordance with UL/CSA requirements.

Mechanical dimensions:
Grid: 2.54mm
Solder pads: 1.6mm
Drill holes: 0.9mm

Fig. 12 Driver module outline