

SINGLE CHANNEL HIGH POWER IGBT-DRIVER-CORE IGD2-3050

FEATURES

- Application for 1200V and 1700V IGBT's
- electrical Isolation test voltage 4000VAC
- Gate currents up to +/-50A
- operating freq. DC to 150kHz
- duty cycle 0 to 100%
- high dv/dt immunity >100.000V/ μ s
- built in isolated DC-DC 15V//+/-15V
- UVLO protection
- 15V trigger Pulse Commands
- isolated Status ACK Pulses

APPLICATIONS

- industrial drives
- railway drives and auxilliaries
- radiology and laser technology
- power engineering

KEY PARAMETERS

- | | |
|-----------------|---------|
| - Input Voltage | 15V |
| - Drive Voltage | +/- 15V |
| - Drive Power | 15W |
| - Gate Drive | +/- 50A |
| - Logic Supply | 15V |
| - Ref.-Voltage | 15V |



IGD2-3050 Application Note

Pin Designation

Pin	Des.	Function	Pin	Des.	Function
1	VDD	+15V electr. input	44	Vpos	+15V block-cap
2	VDD	+15V electr. input	43	COM	out COMMON
3	VDD	+15V electr. input	42	Vneg	-15V block-cap
4	SO	Status Output	41	E	Emitter
5	LLR	Logic Level Reset	40	G	Gate
6	LLI	Logic Level Input	39	E	Emitter
7	GND	Input Ground	38	G	Gate
8	GND	Input Ground	37	E	Emitter
9	GND	Input Ground	36	G	Gate
10	GND	Input Ground	35	ACL*	to be con to Vneg
11	GND	Input Ground	34	Rthr	Reference Res./Z-D.
12	GND	Input Ground	33	C	Collector Sense
13	GND	Input Ground	32	LS	Local Status
14	VDC	+15V supply	31	E	Emitter
15	VDC	+15V supply	30	G	Gate
16	VDC	+15V supply	29	E	Emitter
17	VDC	+15V supply	28	G	Gate
18	VDC	+15V supply	27	E	Emitter
19	VDC	+15V supply	26	G	Gate
20	free		25	Vpos	+15V block-cap
21	VDC	+15V supply	24	COM	out Common
22	VDC	+15V supply	23	Vneg	-15V block-cap

notes:

1. Pin 20 physically not present
2. E (Emitter) is directly connected to COM.
3. Pin 35, Active Clamp (ACL) input
4. VDD & VDC pins are phys. connected

IGD2-3050 IGBT DRIVER

Absolute Maximum Ratings

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

T_{case} = +25°C stated otherwise

Parameter	Test Conditions	Min.	Max.	Units
Supply Voltage VDC		0	16	V DC
Supply Voltage VDD		0	16	V DC
Logic Level Input LLI	to GND	0	VDD	V DC
Logic Level Reset LLR	to GND	0	VDD	V DC
DC-DC Output Power			15	W
I _g peak	G to E	-50	+50	A
max. V operating	continuously		1700	V
isolation test voltage	50Hz / 1 min.		4000	V AC rms
Operating Ambient Temperature		-55	85	°C
Storage Temperature		-55	105	°C
du/dt			100	kV/μs

Electrical Characteristics

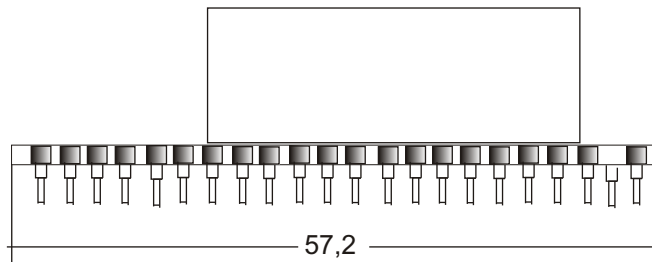
	Test Conditions	Min.	Typ.	Max.	Units
nominal V DC			15		V DC
supply current I DC	without Load		74		mA
max. Supply Current			1200		mA
DC-DC Output Power			15		W
nom. Supply Voltage VDD	GND		15		V
Supply Current IDD	zero load / 50kHz		5 / 20		mA
UVLO		9,9		10,9	V
Logic Level Input LLI & Reset LLR			15		V
Delay time I/O	t _{pd on} t _{pd off}		450 420		ns ns
Output rise/fall time			20/60		ns
Status Output SO current			>20		mA
Local Status LS current			>20		mA

IGD2-3050 IGBT Driver

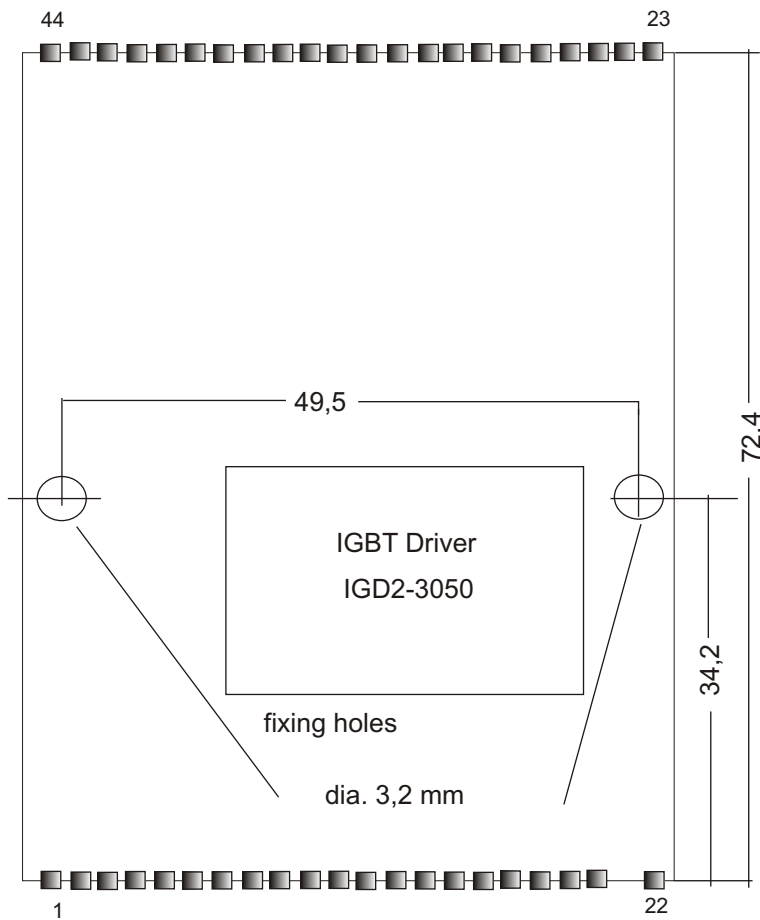
Mechanical Dimensions

Creepage & Clearance I/O > 20mm

Front side View



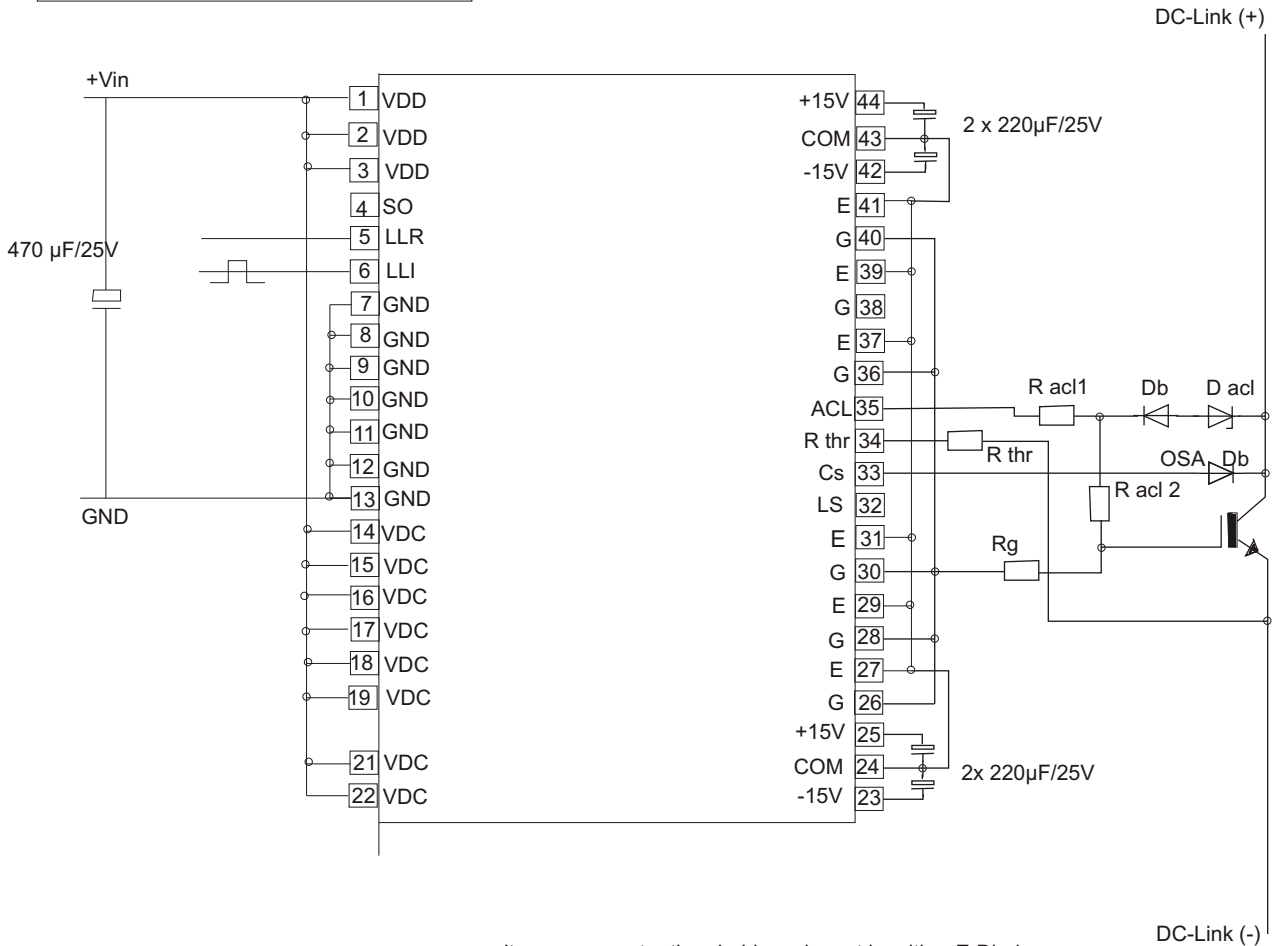
Pin Grid 2,54 mm



Top View

IGD2-3050 IGBT Driver

Application Note Drawing



voltage comparator threshold can be set by either Z-Diode

or proper Resistor gives a stable threshold,
 while Z-voltage drifts with higher temperatures.

To calculate:

$$R_{\text{thres.}} = \frac{56000}{\left[\frac{14,313186}{\text{Comp. Level Value}} - 1 \right]}$$

Pin 4 and Pin 32 are Open Collector taps

Pin 4 Status Output turns LOW in failure mode
 Pin 32 Local Status normal LOW in failure mode HIGH

Pin 5 Logic level Reset
 if LOW driver turns off Output to -15V; trigger level at 3V

IGD2-3050 IGBT Driver

Logic Pin Description

Pin 4 SO Status Output is an OPEN COLL Port
it turns Low in failure mode but ACK pulses appear further

That Port can be resetted by pulling Pin 5 Logic Level Reset LLR to LOW otherwise a periodical continuous retry pushes SO HIGH after 1 sec wait.

Pin 5 Logic Level Reset LLR
pulled LOW - Output will be turned off Gate to -15V, trigger level 3V

Pin 6 Logic Level Input LLI
HIGH at Input generates a Gate HIGH Signal (direct) (none inverting)
Trigger level at 10V

Pin 32 Local Status LS
Normal LOW in failure Mode HIGH after Failure is removed Pin 32 turns after 1 sec. to Low again
and releases the Gate Output for eventual switching.

Out Of Saturation Error OSA
upon error an error flag is generated and upon 1 sec. wait a continuous retry delivers a Gate Signal
if error is not removed it turns off again while when error is removed circuit works orderly.

Status Output SO and Local Status LS can be used upon demand

either bei using a LED-Resistor Network with Cathode to +15V

or wiring them to other control boards.